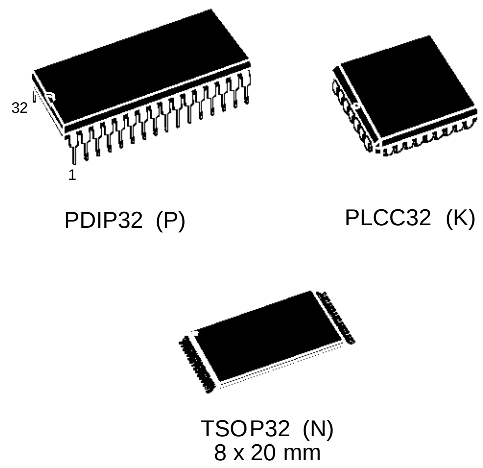
M28F101

1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 70ns
- LOW POWER CONSUMPTION
  – Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- OTP COMPATIBLE PACKAGES and PINOUTS
- EXTENDED TEMPERATURE RANGES



DESCRIPTION

The M28F101 FLASH Memory is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 128K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F101 FLASH Memory is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Figure 1. Logic Diagram

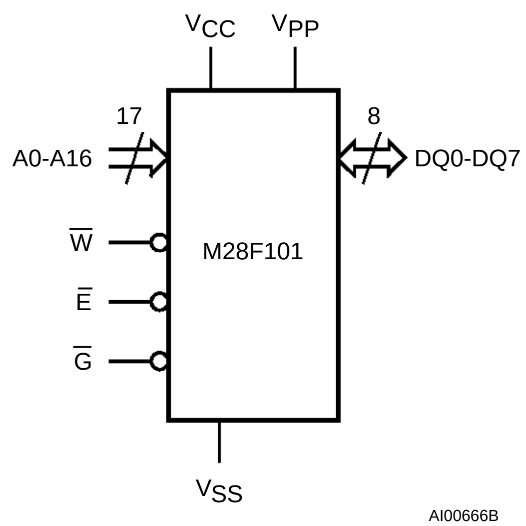
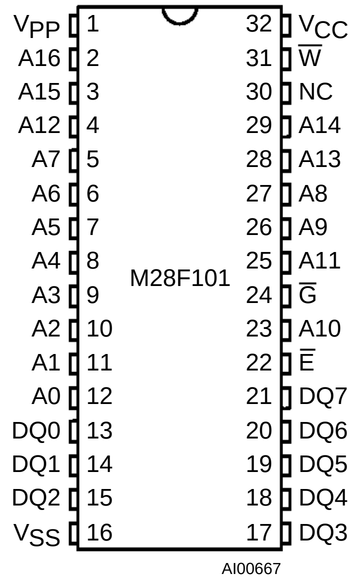


Table 1. Signal Names

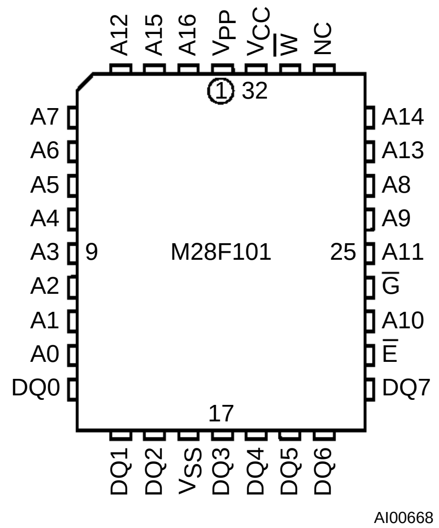
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



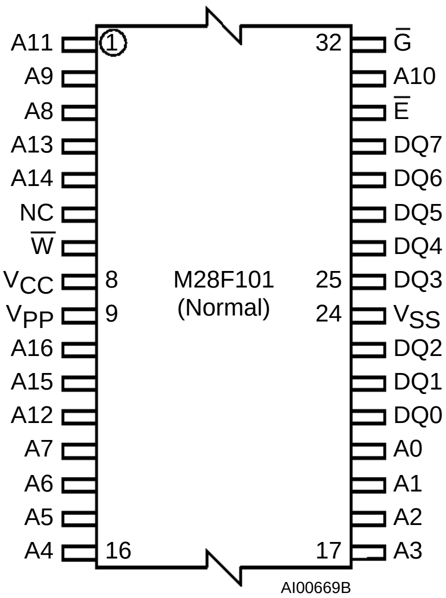
Warning: NC = Not Connected

Figure 2B. LCC Pin Connections



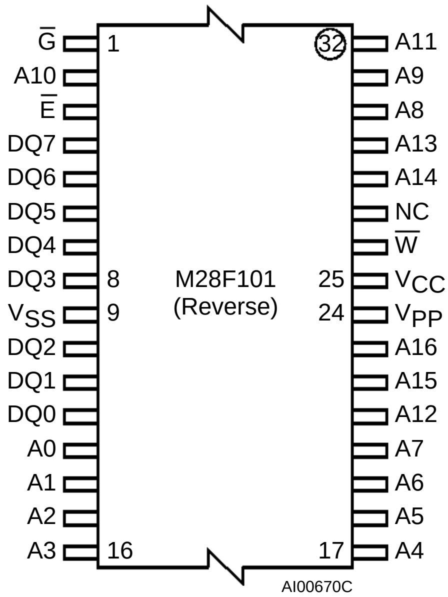
Warning: NC = Not Connected

Figure 2C. TSOP Pin Connections



Warning: NC = Not Connected

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F101 FLASH Memory employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F101 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F101 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A16	DQ0-DQ7	Operation	A0-A16	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	00000h	20h
					Read	00001h	07h
Setup Erase/	2	Write	X	20h			
Erase					Write	X	20h
Erase Verify	2	Write	A0-A16	0A0h	Read	X	Data Output
Setup Program/	2	Write	X	40h			
Program					Write	A0-A16	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is $\leq$ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Table 6. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

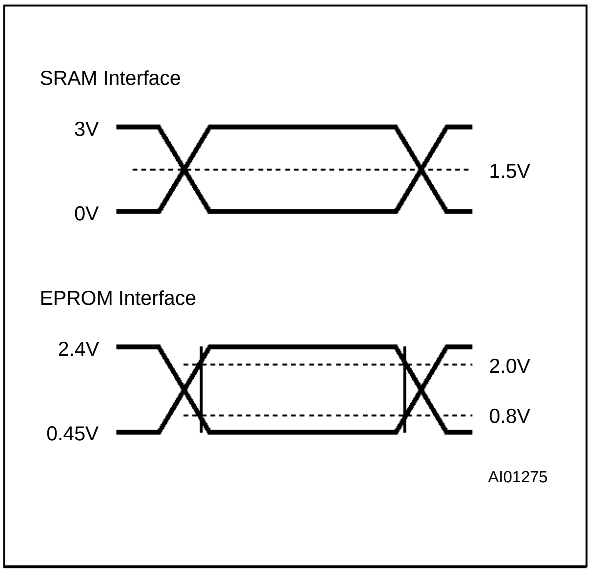


Figure 4. AC Testing Load Circuit

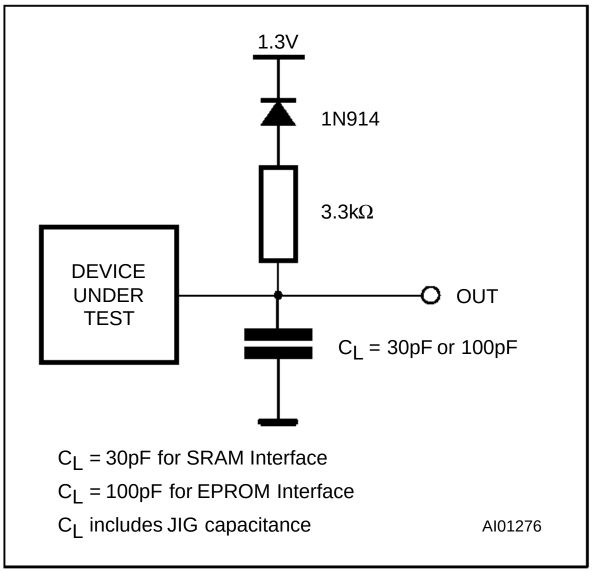


Table 7. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% test.ed

Table 8. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		50	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		15	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		15	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		120	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 9A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101						Unit
				-70		-90		-100		
				V_{CC}=5V±5%		V_{CC}=5V±10%		V_{CC}=5V±10%		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	70		90		100		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		70		90		100	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		70		90		100	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		30		35		45	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	45	0	45	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Table 9B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101						Unit
				-120		-150		-200		
				V_{CC}=5V±10%		V_{CC}=5V±10%		V_{CC}=5V±10%		
				EPROM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh. The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied; reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

Figure 5. Read Mode AC Waveforms

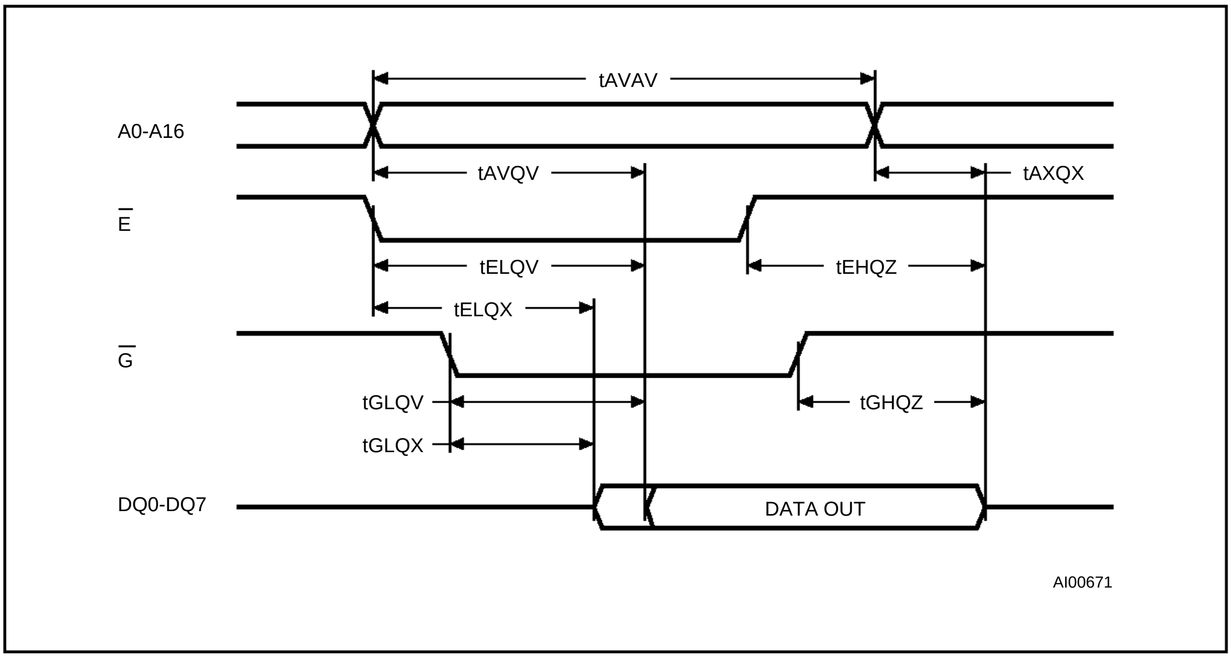


Figure 6. Read Command Waveforms

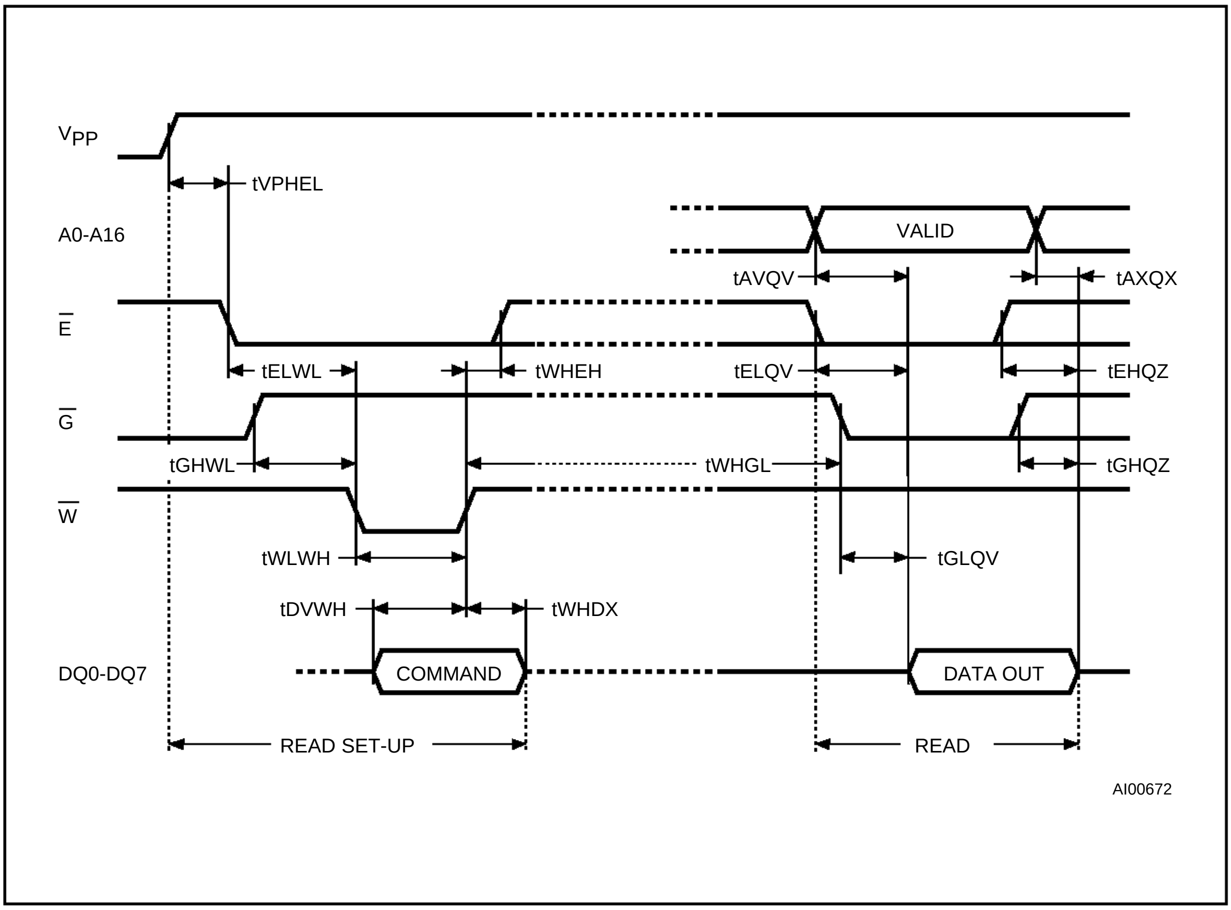
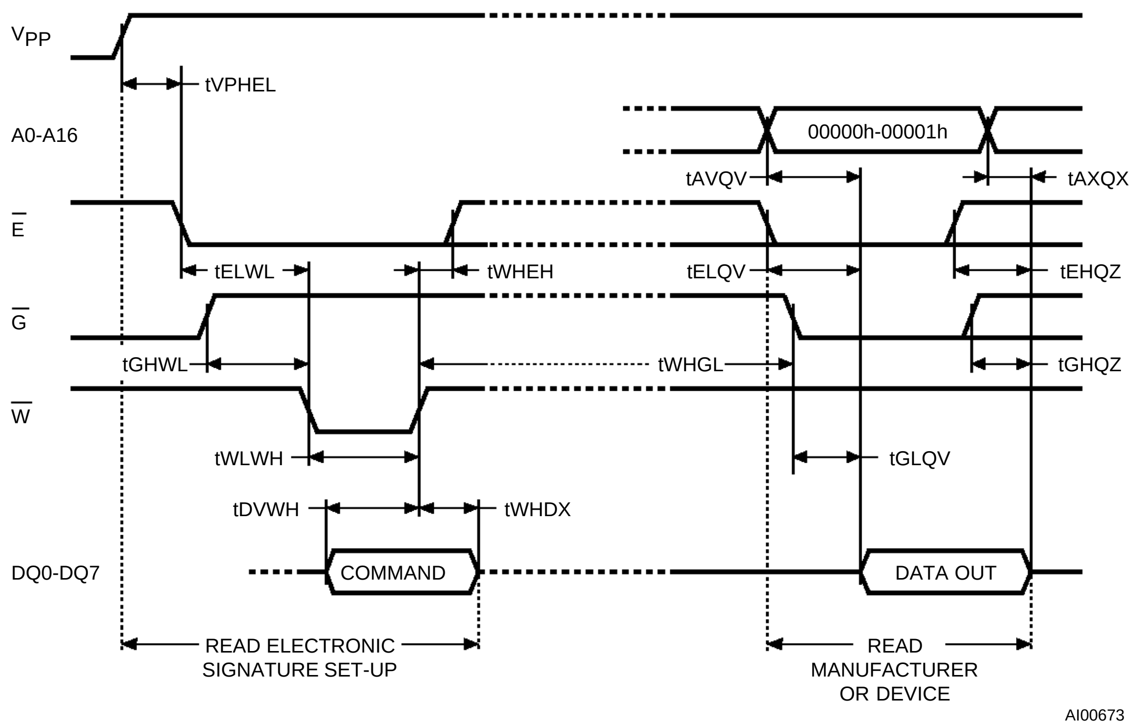


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing 0FFh two times to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 10A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	M28F101						Unit
			-70		-90		-100		
			V_{CC}=5V±5%		V_{CC}=5V±10%		V_{CC}=5V±10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	70		90		100		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	40		40		40		ns
t_{ELAX}		Chip Enable Low to Address Transition	50		60		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	10		15		15		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		40		40		ns
t_{DVEH}		Input Valid to Chip Enable High	30		35		40		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	35		40		40		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	35		45		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		70		90		100	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		70		90		100	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		30		35		45	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		30		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 10B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	M28F101 -120 V_{CC}=5V±10% EPROM Interface Min	-120 Max	-150 V_{CC}=5V±10% EPROM Interface Min	-150 Max	-200 V_{CC}=5V±10% EPROM Interface Min	-200 Max	Unit
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		120		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		50		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		50		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms, $\overline{W}$ Controlled

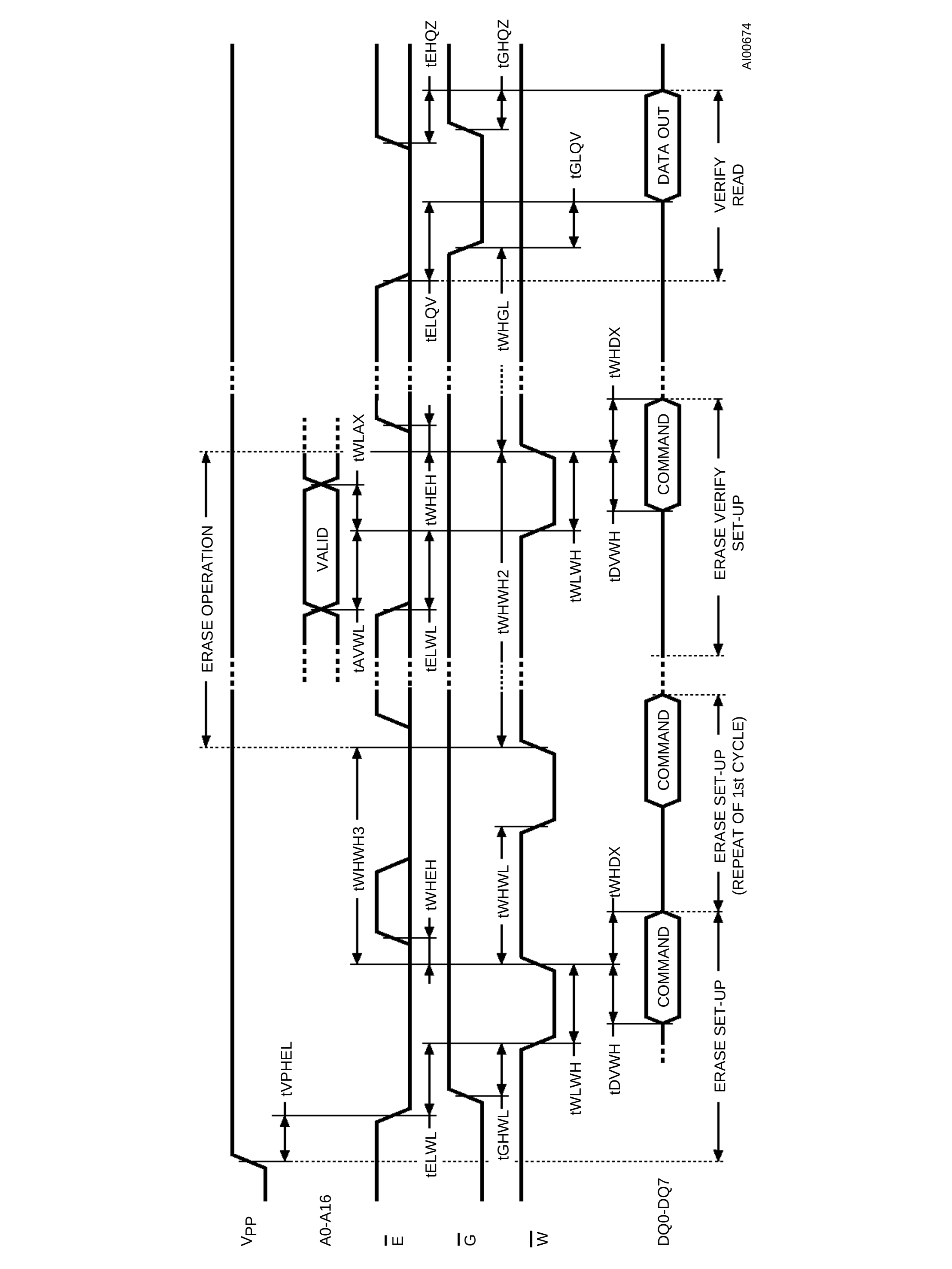


Figure 9. Erase Set-up and Erase Verify Commands Waveforms, $\overline{E}$ Controlled

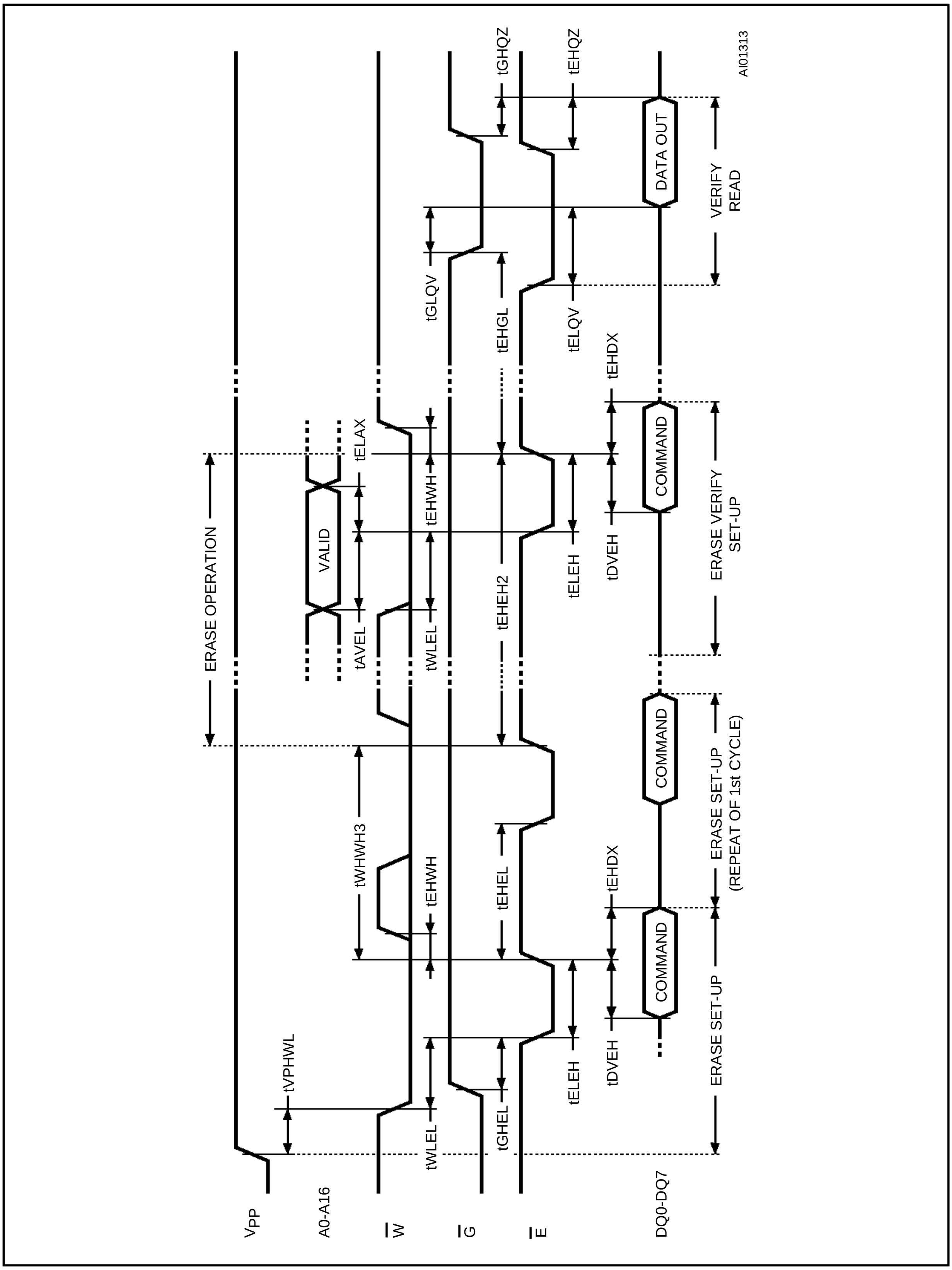


Figure 10. Program Set-up and Program Verify Commands Waveforms, $\overline{W}$ Controlled

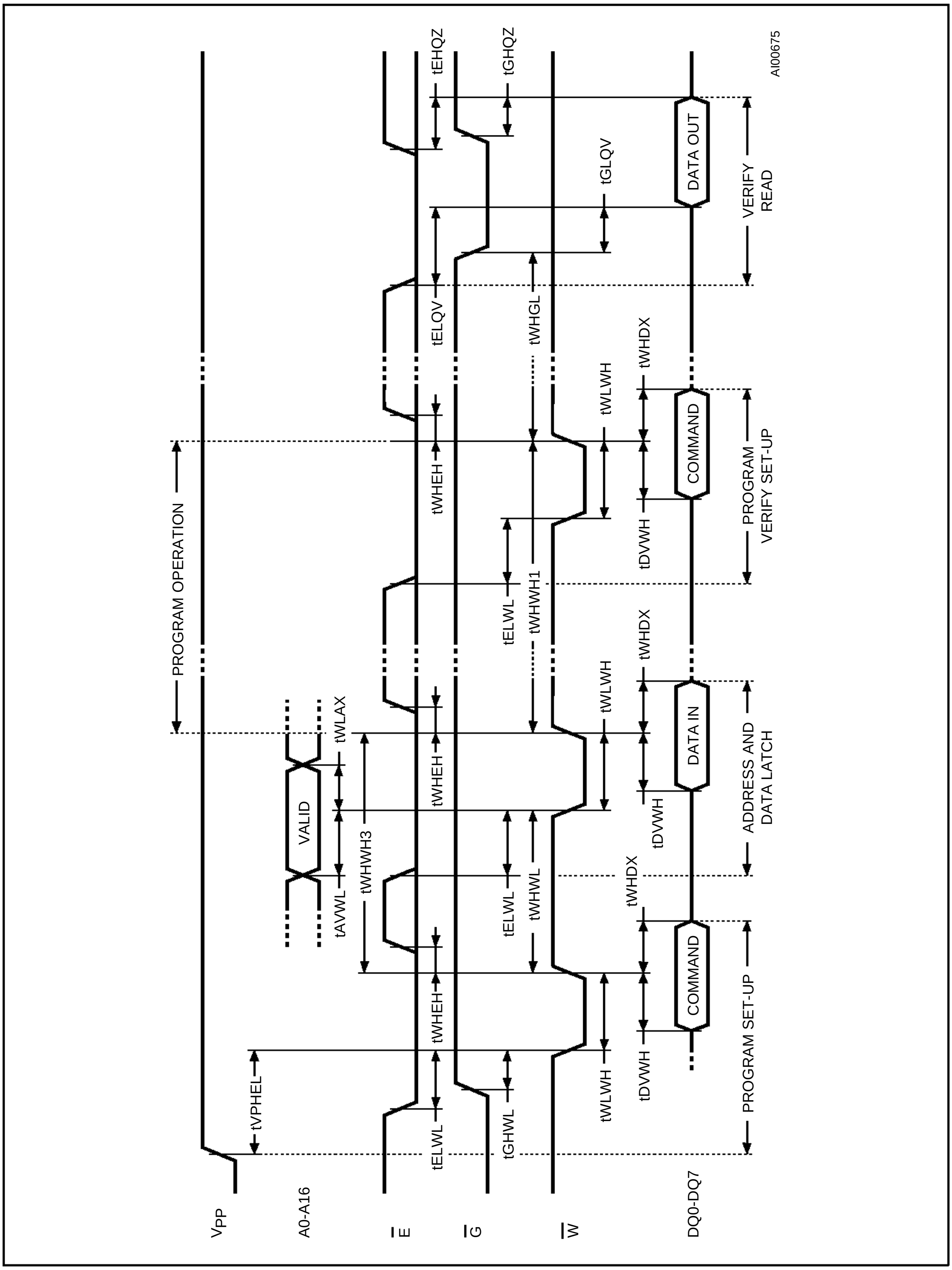


Figure 11. Program Set-up and Program Verify Commands Waveforms, $\overline{E}$ Controlled

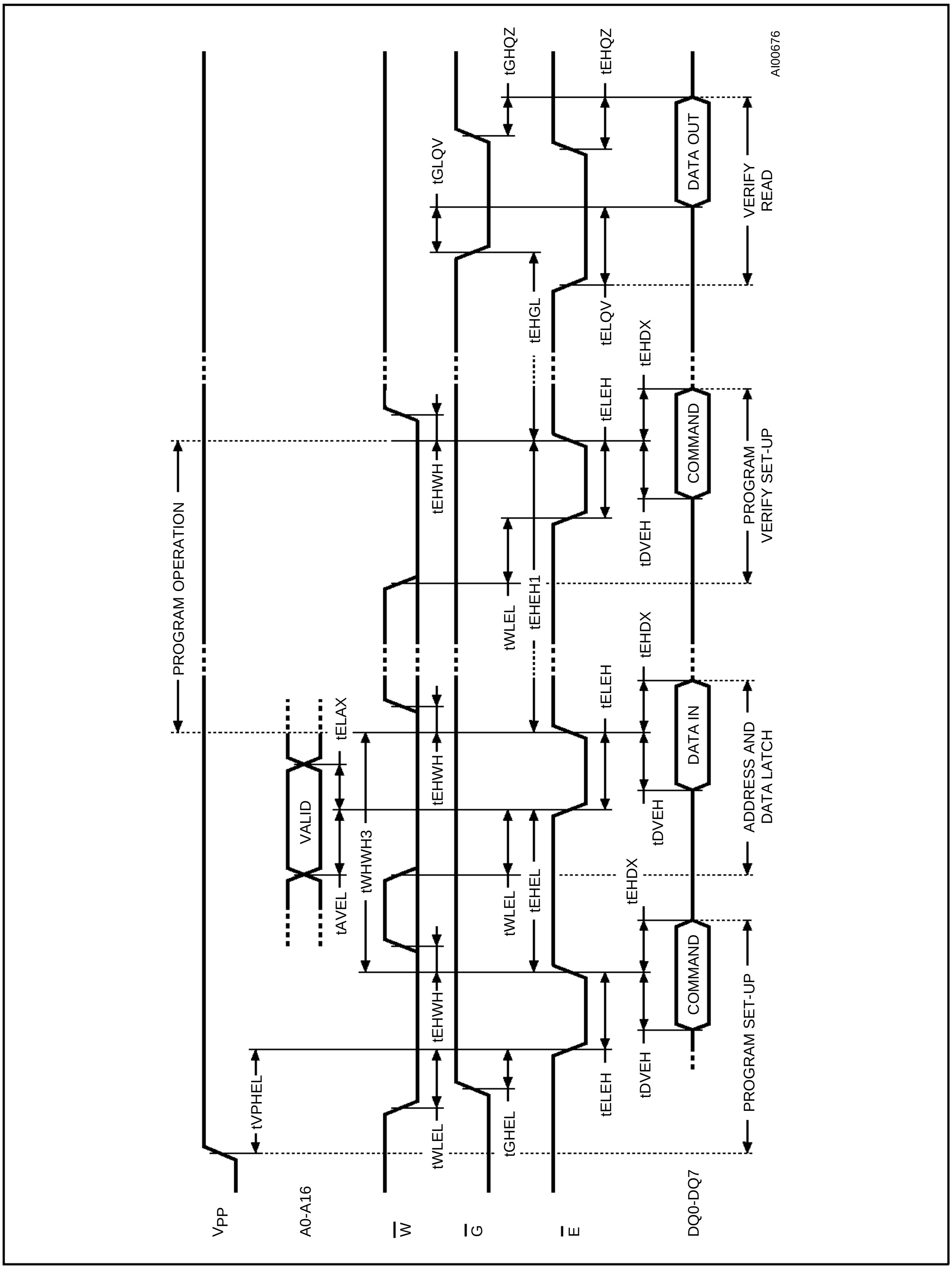
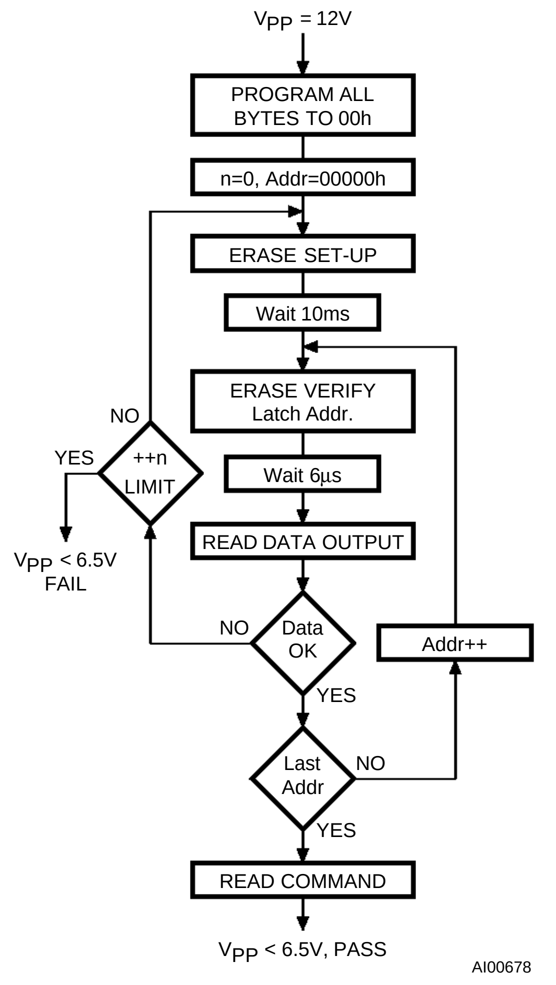
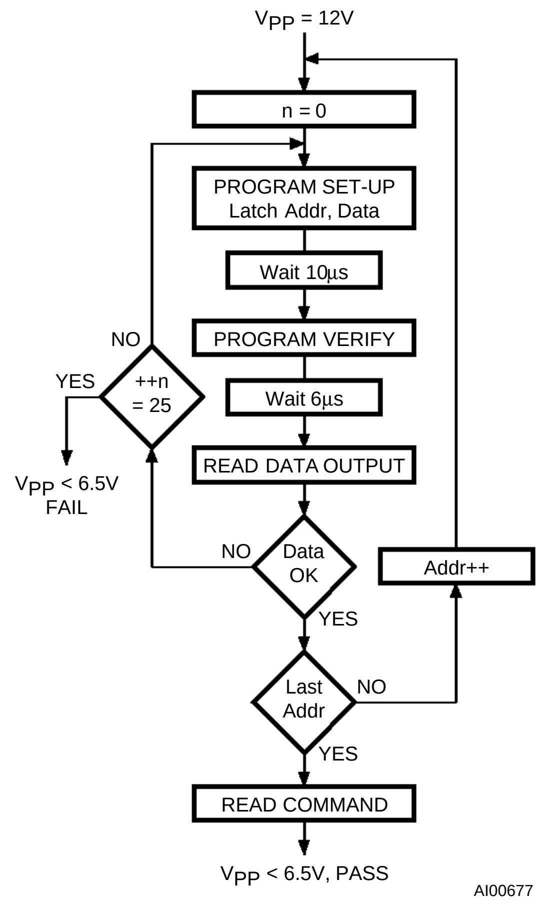


Figure 12. Erasing Flowchart



Limit: 1000 at grade 1; 6000 at grades 3 & 6.

Figure 13. Programming Flowchart



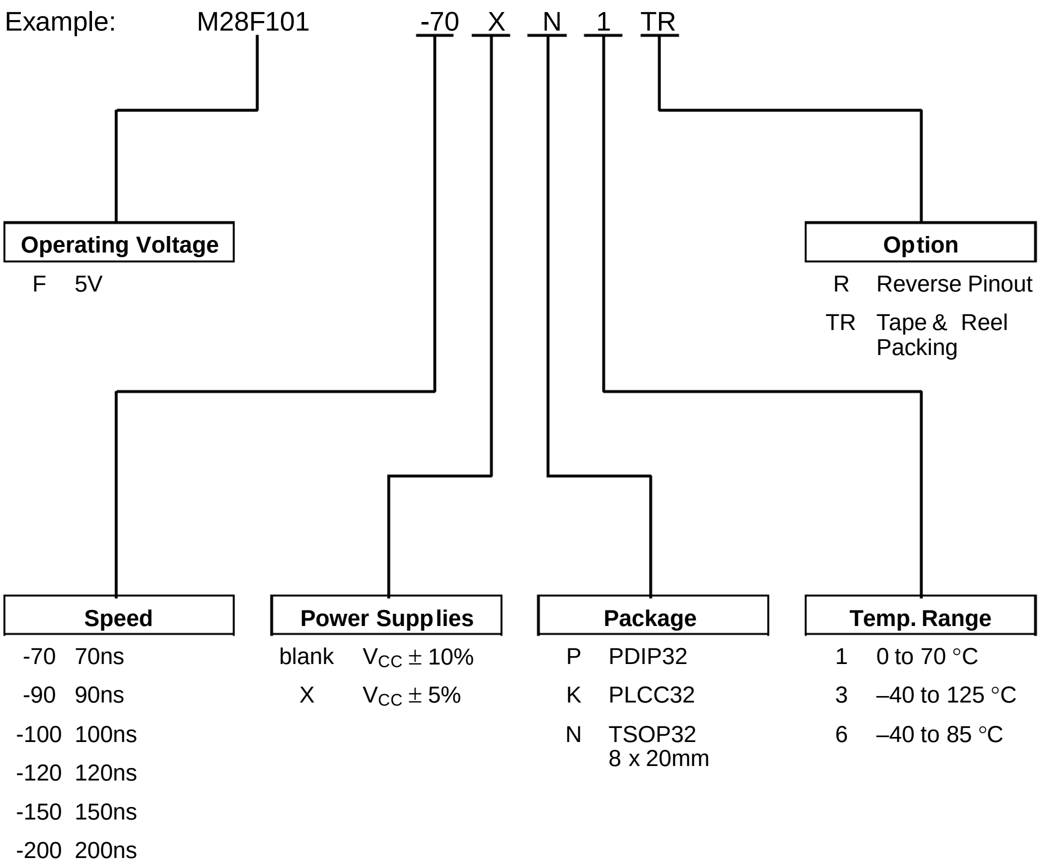
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME



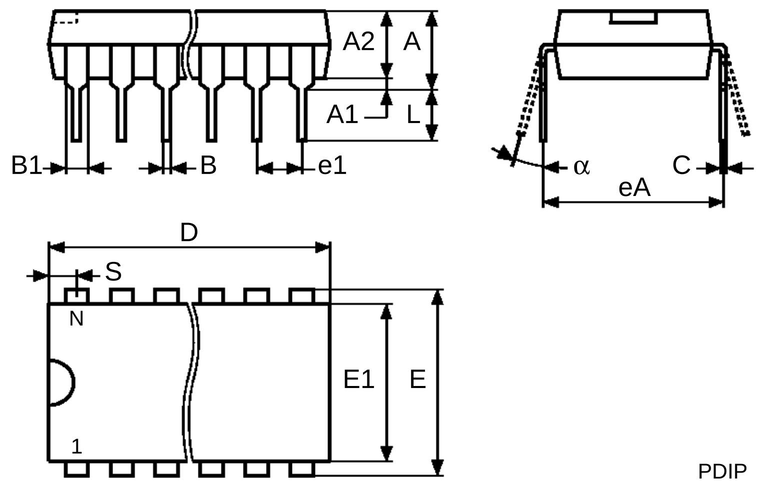
For a list of available options (V_{CC} Range, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32

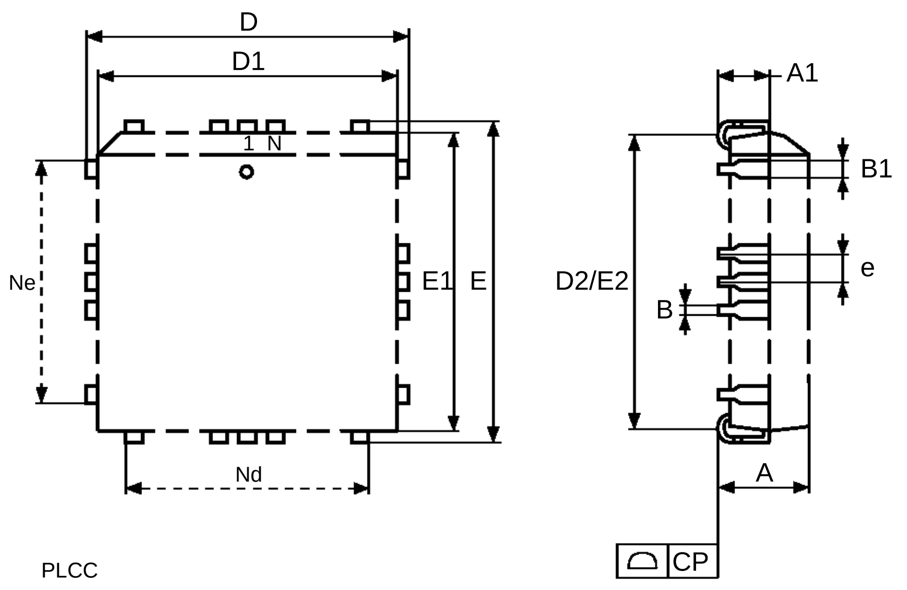


Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



PLCC

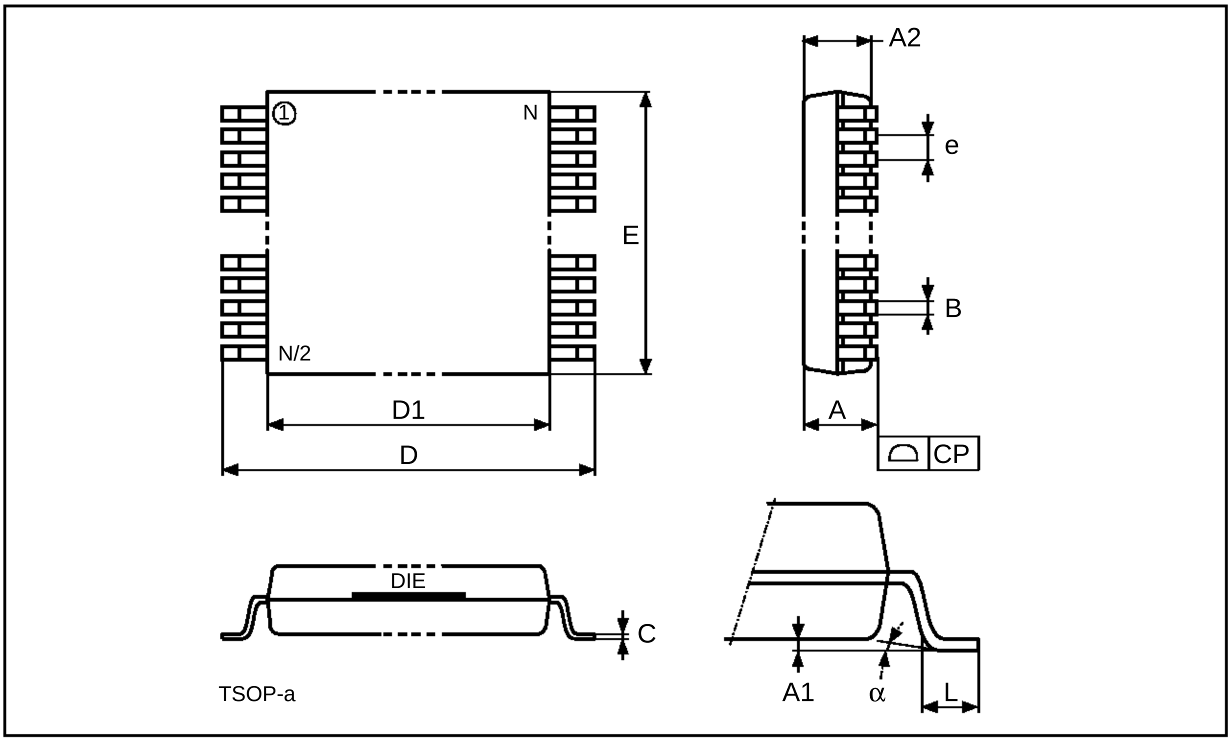
Drawing is not to scale

SGS-THOMSON MICROELECTRONICS

TSOP32 Normal Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.04	1.24		0.041	0.049
A1		0.05	0.20		0.002	0.008
A2		0.95	1.06		0.037	0.042
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.90	20.12		0.783	0.792
D1		18.24	18.49		0.718	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

TSOP32

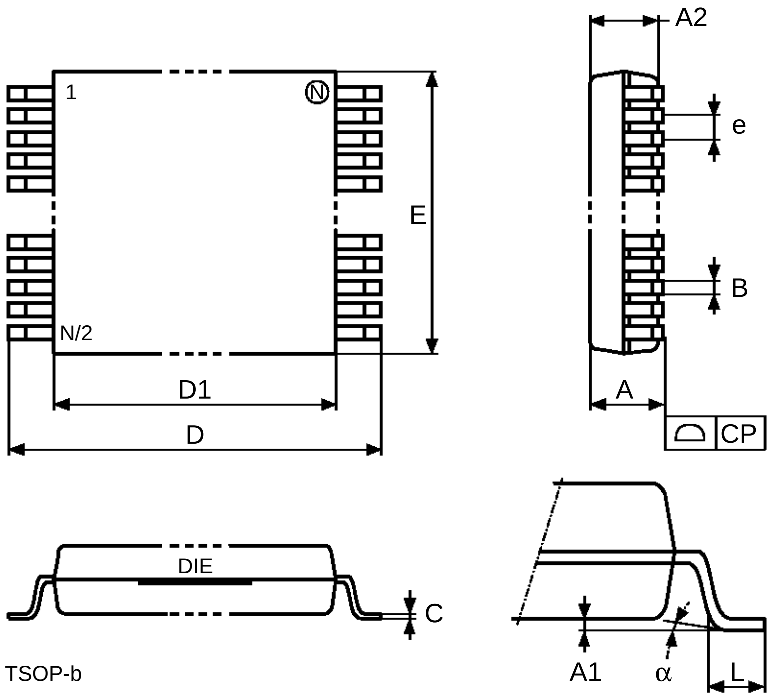


Drawing is not to scale

TSOP32 Reverse Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.04	1.24		0.041	0.049
A1		0.05	0.20		0.002	0.008
A2		0.95	1.06		0.037	0.042
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.90	20.12		0.783	0.792
D1		18.24	18.49		0.718	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

TSOP32



TSOP-b

Drawing is not to scale